IN THE SPECIFICATION

Please amend the Specification as follows:

Before paragraph no. [0035], beginning at page 9, line 6, please add the following paragraph:

"Innovative routing methods for an integrated circuit design layout are disclosed. The integrated circuit design layout can include design netlists and library cells. A multiple-level global routing can generate a topological wire for each net. An area oriented graph-based detailed routing on the integrated circuit design layout can be performed. A post route optimization can be performed after the detailed routing to further improve the routing quality of the integrated circuit design layout. The routing methods may be single threaded all or some of the time, and/or multi-threaded some or all of the time."

Please amend paragraph no. [0037] beginning at page 9, line 24, as follows:

"Referring now to FIG. 2, subsystems of a routing engine 200 are illustrated. The routing engine 200 comprises a multi-level area-based global router 201 and a graph-based detail router 202. Some embodiments of the multi-level global router 201 construct multiple levels each

with a global routing grid covering the entire IC design of one or more layers. The global router 201 receives a design netlist 210. At any one moment, only a portion, such as an area of one or more partitions, of the design is routed; therefore much less memory and run time are required. Some embodiments route portions having a size of a partition. In addition, since the routing task has been divided, multi-threaded parallelism can be applied to speed up the global router 201. At this stage, the global router 201 generates topological wiring 220, which is passed on to the detail router 202. To generate the physical wires 230 which realize the topological wiring 220, the detail router 202 routes the complete design by dividing the entire design into a set of smaller areas and/or partitions. The detail router 202 can route these areas in parallel utilizing the multi-threaded parallel computing capability of some embodiments of the present invention. Other embodiments can be single threaded all or some of the time, and/or multi-threaded all or some of the time."

Before paragraph no. [0051], beginning at page 14, line 10, please add the following paragraph:

"FIG. 6 illustrates a graph representation in a given routing area avoiding or decreasing nodes on blockages.

Five metal wire routing layers, metal 1, metal 2, metal 3, metal 4, and metal 5, are illustrated for interconnecting graph nodes in the given routing area.

Please amend paragraph no. [0051] beginning at page 14, line 10, as follows:

"In FIG. 6, there is a big blockage 610 inside the routing area. In grid based routing, the entire area [[will]] would be covered by a grid, regardless of the fact that there exists a big blockage. This is due to the uniform structure requirement of the grid representation. In a graph representation, ~~the figure~~ FIG. 6 shows that we can construct graph nodes [[only]] for the empty space unoccupied by the blockage 610, without creating graph nodes for the blockage. The resulting graph has fewer nodes since much of the space is occupied by the blockage 610. By using the graph representation, the number of graph nodes is much smaller than the number of [[grid]] grids and therefore [[have]] has a significant memory reduction compared to a grid representation. In addition, the graph-based routing algorithm has fewer nodes to traverse and hence reduce significant CPU time. In other embodiments, the number of nodes in or around a blockage is at least reduced compared

to a grid representation, without reducing the number of nodes in or around the blockage to zero."

Please amend paragraph no. [0057] beginning at page 16, line 11, as follows:

"Some embodiments ~~interconnected~~ interconnect at least a first portion of the IC design at a first routing pitch. If interconnecting results in one or more design rule violations, at least a part of the first portion of the IC design is routed at a second routing pitch differing from and maybe greater than or less than the first routing pitch."